The opinion in support of the decision being entered today was  $\underline{not}$  written for publication and is  $\underline{not}$  binding precedent of the Board.

Paper No. 15

#### UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MICHAEL N. MISHELOFF and PAUL R. FINDLEY

\_\_\_\_\_

Appeal No. 2002-0550 Application 09/264,770

\_\_\_\_\_

ON BRIEF

\_\_\_\_\_

Before THOMAS, HAIRSTON, and FLEMING, <u>Administrative Patent</u> <u>Judges</u>.

HAIRSTON, Administrative Patent Judge.

### DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 21.

The disclosed invention relates to a method for producing a logic cell.

Appeal No. 2002-0550 Application No. 09/264,770

Claim 1 is illustrative of the claimed invention, and it reads as follows:

- 1. A method for producing a logic cell, the method comprising the following steps:
- (a) generating a timing model for the logic cell, including the following substeps:
- (a.1) selecting output load indices (Load<sub>1</sub>, Load<sub>2</sub>,..., Load<sub>m</sub>) which specify output load for the first logic cell,
- (a.2) selecting input ramp indices (IR<sub>1</sub>, IR<sub>2</sub>, ..., IR<sub>n</sub>) which specify input ramp for the first logic cell,
- (a.3) generating baseline output ramp values ( $OR_{b1}[j,k]$ ) for each output load index ( $Load_j$ ) and input ramp index ( $IR_K$ ) pair,
- (a.4) scaling the output load indices by a first scaling factor  $(\boldsymbol{\lambda})\,\text{,}$
- (a.5) scaling the input ramp indices by a second scaling factor  $(\rho)$ , and
- (a.6) generating scaled output ramp values ( $OR_{scaled}$  [j,k]) for each scaled output load index and scaled input ramp index pair, wherein a numerical value of  $OR_{scaled}$  [j,k] represents a value of output ramp at new Process, Power supply, Temperature conditions when the output load for the first logic cell is equal to  $\Lambda^*$  Load<sub>j</sub> and the input ramp for the first logic cell is equal to  $\rho^*$  IR<sub>k</sub>; and,
- (b) building the logic cell based on the timing model generated in step (a).

The references relied on by the examiner are:

Misheloff 5,559,715 Sept. 24, 1996 McNelly et al. (McNelly) 5,625,803 Apr. 29, 1997

Claims 1 through 21 stand rejected under 35 U.S.C. § 102(b) as being anticipated by either the admitted prior art, McNelly or Misheloff.

Reference is made to the final rejection (paper number 6), the brief (paper number 10) and the answer (paper number 11) for the respective positions of the appellants and the examiner.

#### OPINION

We have carefully considered the entire record before us, and we will reverse the anticipation rejection of claims 1 through 21.

Anticipation is only established when a single prior art reference discloses every limitation of the claimed invention, either explicitly or inherently. Glaxo Inc. v. Novopharm Ltd., 52 F.3d 1043, 1047, 34 USPQ2d 1565, 1567 (Fed. Cir. 1995), cert. denied, 516 U.S. 988. The examiner has made findings (final rejection, pages 4 and 5) that the admitted prior art, McNelly and Misheloff disclose all of the limitations of claims 1 through 21. Appellants argue (brief, pages 23 through 32) that substeps (a.4) through (a.6) of the claimed invention are not disclosed in the admitted prior art or the references to McNelly and Misheloff, and that the examiner has not presented a sufficient demonstration of how the claimed invention reads on the admitted

Appeal No. 2002-0550 Application No. 09/264,770

prior art, McNelly and Misheloff to justify an anticipation rejection.

We agree with appellants' arguments. The mere fact that the admitted prior art "discloses a prior art teaching of the incorporation of P, V, T variations using scaling factors" (final rejection, page 4) does not necessarily mean that the admitted prior art teaches a method of producing a logic cell in the manner set forth in substeps (a.4) through (a.6) of the claimed invention. The rejection lacks a showing as to how the teachings of the admitted prior art anticipates the six substeps of the claimed invention. With respect to the teachings of the two applied references, the examiner has reproduced the abstracts from each reference verbatim in the rejection (final rejection, pages 4 and 5), and noted several columns and lines in each reference for review (final rejection, page 5). We have reviewed the abstracts in the two references, and the referenced columns and lines in each reference, and we can not find any disclosure of the claimed method substeps (a.4) through (a.6) in such teachings.

In view of the foregoing, the anticipation rejection of claims 1 through 21 is reversed because the examiner has not made a prima facie showing of anticipation.

Application No. 09/264,770

## **DECISION**

The decision of the examiner rejecting claims 1 through 21 under 35 U.S.C. § 102(b) is reversed.

# REVERSED

JAMES D. THOMAS Administrative Patent	Judge	)
KENNETH W. HAIRSTON Administrative Patent	Judge	) ) BOARD OF PATENT ) APPEALS AND ) INTERFERENCES ) )
MICHAEL R. FLEMING Administrative Patent	Judge	) ) )

KWH:dal

Appeal No. 2002-0550 Application No. 09/264,770

CORPORATE PATENT COUNSEL
PHILIPS ELECTRONICS NORTH AMERICA
CORPORATION
580 WHITE PLAINS ROAD
TARRYTOWN NY 10591